In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method of fabricating an integrated circuit on a substrate, comprising:

(a) providing a semiconductor substrate with a dielectric layer formed thereon;

(b) forming an electroconductive layer on said dielectric layer;

(c) forming a pattern comprised of an opening in said electroconductive layer that extends through said dielectric layer;

(d) depositing a diffusion barrier layer on said electroconductive layer and within said opening;

(e) depositing a metal seed layer on said diffusion barrier layer;

(f) removing said metal seed layer above said electroconductive layer by a first planarization process; ~~and~~

(g) forming a metal layer on the metal seed layer by a selective electrochemical deposition to fill said opening and

(h) performing a second planarization process so that said metal layer becomes coplanar with said dielectric layer.

2. (canceled)

3. (original) The method of claim 1 wherein the dielectric layer is comprised of a low k dielectric material that is fluorine doped Si02, carbon doped Si02, nitrogen doped SiO_2, borophosphosilicate glass, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or a fluorinated polyimide and has a thickness of about 1000 to 10000 Angstroms.

4. (original) The method of claim 1 wherein said opening has a width of about 200 nm or less.

5. (original) The method of claim 1 wherein said electroconductive layer is selected from a group of materials including W, Al, WN, Ti, and TiN.

6. (original) The method of claim 1 wherein said electroconductive layer is a metal compound, a metal alloy, or an amorphous metal that is a good electrical conductor and which can function as a stop layer in a copper CMP process and as a hard mask during an oxygen based plasma etch to form said opening.

7. (original) The method of claim 1 wherein said electroconductive layer has a thickness in the range of about 50 to 1000 Angstroms.

8. (original) The method of claim 1 wherein said electrochemical layer is formed by a physical vapor deposition (PVD) or chemical vapor deposition (CVD) process.

9. (original) The method of claim 4 wherein said opening is formed by patterning a photoresist layer on the electroconductive layer and transferring said opening through the electroconductive layer and dielectric layer by one or more plasma etch steps.

10. (original) The method of claim 1 wherein said substrate is further comprised of a conductive layer and an etch stop layer formed on said conductive layer.

11. (original) The method of claim 10 wherein the opening in said dielectric layer is transferred through said etch stop layer by a plasma etch step to expose a portion of said conductive layer before the diffusion layer is deposited.

12. (original) The method of claim 1 wherein said diffusion barrier layer has a thickness of about 20 to 500 Angstroms and is deposited by a CVD, plasma enhanced CVD (PECVD), PVD, or atomic layer deposition (ALD) technique.

13. (original) The method of claim 1 wherein said metal seed layer is a copper layer with a thickness of about 10 to 1000 Angstroms and is deposited by a PVD, CVD, or ALD process.

14. (currently amended) The method of claim ~~2~~ 1 wherein first and second planarization processes are accomplished by a chemical mechanical polish (CMP) process.

15. (original) The method of claim 1 wherein the first planarization process removes the diffusion barrier layer and metal seed layer above said electroconductive layer.

16. (original) The method of claim 15 wherein said electroconductive layer has a polish rate that is lower than said diffusison barrier layer and functions as a CMP stop layer.

17. (original) The method of claim 1 wherein said metal layer is copper.

18. (original) A method of forming a uniform copper interconnect layer on a substrate, comprising:

(a) providing a substrate having a stack of layers formed thereon, said stack is comprised of a bottom etch stop layer, a middle dielectric layer, and an upper electroconductive layer;

(b) forming a pattern comprised of an opening in said electroconductive layer that extends through said dielectric layer and said etch stop layer;

(c) depositing a diffusion barrier layer on said electroconductive layer and within said opening;

(d) depositing a copper seed layer on said diffusion barrier layer;

(e) removing said copper seed layer above said electroconductive layer by a first planarization process;

(f) forming a copper layer on the copper seed layer by a selective electrochemical deposition to fill said opening; and

(g) performing a second planarization process so that said copper layer becomes coplanar with said dielectric layer.

19. (original) The method of claim 18 wherein the dielectric layer is comprised of a low k dielectric material that is fluorine doped SiO2, carbon doped SiO_2, nitrogen doped SiO2, borophosphosilicate glass, a poly(arylether), a polysilsesquioxane, benzocyclobutene, or a fluorinated polyimide and has a thickness of about 1000 to 10000 Angstroms.

20. (original) The method of claim 18 wherein said opening has a width of about 200 nm or less.

21. (original) The method of claim 18 wherein said electroconductive layer is selected from a group of materials including W, AI, WN, Ti, and TiN.

22. (original) The method of claim 18 wherein said electroconductive layer is a metal compound, a metal alloy, or an amorphous metal that is a good electrical conductor and which can function as a stop layer in a copper CMP planarization process an~ as a hard mask during an oxygen based plasma etch to form said opening.

23. (original) The method of claim 18 wherein said electroconductive layer has a thickness in the range of about 50 to 2000 Angstroms.

24. (original) The method of claim 18 wherein said electroconductive layer is formed by a PVD or CVD process.

25. (original) The method of claim 18 wherein said opening is formed by patterning a photoresist layer on the electroconductive layer and transferring said opening through the electroconductive layer, dielectric layer, and etch stop layer by one or more plasma etch steps.

26. (original) The method of claim 18 wherein said substrate is further comprised of a conductive layer and wherein said opening exposes a portion of said conductive layer.

27. (original) The method of claim 18 wherein said diffusion barrier layer has a thickness of about 20 to 500 Angstroms and is deposited by a CVD, plasma enhanced CVD, PVD, or ALD technique.

28. (original) The method of claim 18 wherein said copper seed layer is deposited by a PVD CVD, or ALD process.

29. (original) The method of claim 18 wherein said first and second planarization processes comprise a CMP process.

30. (original) The method of claim 18 further comprised of removing said diffusion barrier layer above said electroconductive layer during said first planarization process.

31. (original) The method of claim 30 wherein said electroconductive layer has a polish rate that is lower than said diffusion barrier layer and functions as a CMP stop layer.

32. (original) The method of claim 18 wherein said electroconductive layer and the top portions of said diffusion barrier layer and copper seed layer in said opening are removed during said second planarization process to yield a uniform thickness of said copper layer within said opening.

33. (original) The method of claim 18 wherein said pattern is further comprised of other openings and a uniform copper wiring thickness is formed within all openings in said pattern.